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Title: JP7249403A2: LAYERED BATTERY AND MANUFACTURE THEREOF

Country: JP Japan

Kind: A

Inventor: YOSHIHISA HIROYOSHI;

Assignee: YUASA CORP
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Published / Filed: 1995-09-26 / 1994-03-11

Application Number: JP1994000040243

IPC Code: H01M 2/34; H01M 2/18; H01M 6/18;

Priority Number: 1994-03-11 JP1994000040243

Abstract:

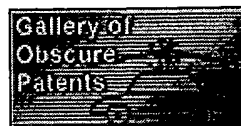
... PURPOSE: To increase position accuracy and prevent internal short circuit to improve reliability and mass productivity by providing electric insulating layers in the peripheral edge parts of positive or negative electrodes to form the positive electrodes and solid electrolyte films to them by coating or a printing method.

... CONSTITUTION: Unhardened paste, wherein active material and a conductive agent are mixed with a high molecular solid electrolyte, is applied by coating or printing onto the aluminium foil 2 of a positive electrode collector, and then is hardened to form a positive electrode 1. Like the positive electrode 1, the same paste is applied onto the positive electrode 1 to be hardened to form a high molecular solid electrolyte film 3, and a negative electrode 4 composed of lithium foil is pressed onto the copper foil 5 of a negative electrode collector. Then a window-like electric insulating layer 6 is coated on the peripheral edge part of the foil 2 to be formed slightly larger than the positive electrode 1 and the film 3 to insert the negative electrode 4 in the window frame of the layer 6. These are enclosed in casings 7 and 8 of stainless foil doubling as the negative and positive electrodes to be fusedly sealed by sealing resin 9. Consequently, position accuracy can be increased to prevent internal short circuit to increase reliability and mass productivity.

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Family: None

Other Abstract Info: CHEMABS 124(02)012354K CAN124(02)012354K DERABS C95-370211 DERC95-370211



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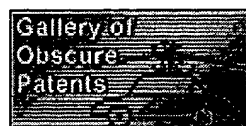
Get Now: ☒ PDF | [More choices...](#)Tools: Add to Work File: [Create new Wor](#)View: [INPADOC](#) | Jump to: [Top](#)  Go to: [Derwent...](#)[Email](#)**Title:** JP7249403A2: LAYERED BATTERY AND MANUFACTURE THEREOF**Country:** JP Japan**Kind:** A**Inventor:** YOSHIHISA HIROYOSHI;**Assignee:** YUASA CORP
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(19)

(11) Publication number: **07**

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PATENT ABSTRACTS OF JAPAN(21) Application number: **06040243**(51) Intl. Cl.: **H01M 2/34 H01M 2/18 H01M**(22) Application date: **11.03.94**

(30) Priority:

(43) Date of application
publication: **26.09.95**(84) Designated contracting
states:(71) Applicant: **YUASA CORP**(72) Inventor: **YOSHIHISA HIROYOSH**

(74) Representative:

**(54) LAYERED BATTERY
AND MANUFACTURE
THEREOF**

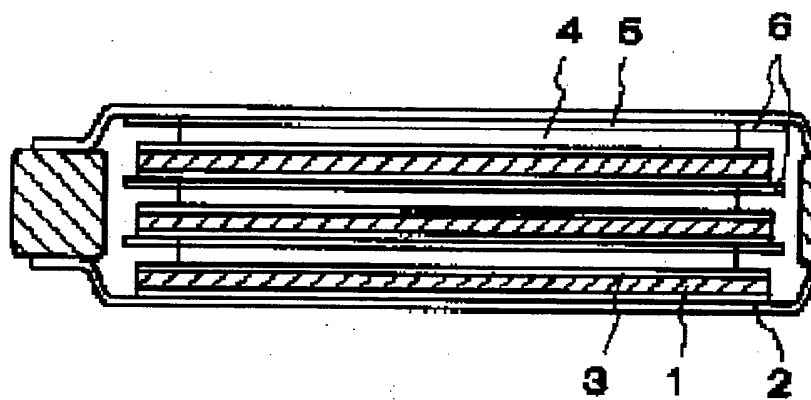
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